What is claimed is

1. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting means for detecting, with specified timing, a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging means for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting means; and

a timing stopping means for stopping said timing of detecting said predetermined frame synchronization pattern only for a specified period of time before and after a frame pulse is generated which indicates a head of a frame containing said received data when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging means.

2. The frame synchronization detecting circuit according to Claim 1, further comprising a resetting means for resetting frame synchronization detecting operations to be performed by said frame synchronization pattern detecting means and said hunting state judging means at a time other than said specified period of time before and after said frame pulse is generated when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging means.

3. The frame synchronization detecting circuit according to Claim 2, wherein said stopping by said timing stopping means and said resetting by said resetting means are performed with different timing.

4. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting means for detecting a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging means for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting means; and

a received data fixing means for making said received data fixed only for a specified period of time before and after a frame pulse is generated which indicates a head of a frame containing said received data when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging means.

5. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting means for detecting a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging means for judging whether said frame synchronization detecting circuit is in a hunting state in which

said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting means; and

a resetting means for resetting frame synchronization detecting operations to be performed by said frame synchronization pattern detecting means and said hunting state judging means at a time other than said specified period of time before and after said frame pulse is generated when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging means.

6. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting means for detecting a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging means for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting means; and

a circuit stop controlling means for stopping an operation of a circuit connected to a front stage only for a specified period of time before and after a frame pulse is generated when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging means.

7. The frame synchronization detecting circuit according to Claim 6, wherein said circuit stop controlling means,

when canceling a stop of operations of said circuit, cancels said stop of operations of said circuit connected to said front stage after it has canceled a stop of timing of frame synchronization detection operations.

8. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting means for detecting a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging means for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting means; and

a circuit operation stopping means for stopping operations of, at least, a part of said frame synchronization detecting circuit only for a specified period of time before and after a frame pulse is generated which indicates a head of a frame containing said received data when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging means.

9. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting circuit for detecting, with specified timing, a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging circuit for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting circuit; and

a timing stopping circuit for stopping said timing of detecting said predetermined frame synchronization pattern only for a specified period of time before and after a frame pulse is generated which indicates a head of a frame containing said received data when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging circuit.

10. The frame synchronization detecting circuit according to Claim 9, further comprising a resetting circuit for resetting frame synchronization detecting operations to be performed by said frame synchronization pattern detecting circuit and said hunting state judging circuit at a time other than said specified period of time before and after said frame pulse is generated when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging circuit.

11. The frame synchronization detecting circuit according to Claim 10, wherein said stopping by said timing stopping circuit and said resetting by said resetting circuit are performed with different timing.

12. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting circuit for detecting a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging circuit for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting circuit; and

a received data fixing circuit for making said received data fixed only for a specified period of time before and after a frame pulse is generated which indicates a head of a frame containing said received data when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging circuit.

13. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting circuit for detecting a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging circuit for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting circuit; and

a resetting circuit for resetting frame synchronization detecting operations to be performed by said frame synchronization pattern detecting circuit and said hunting state judging circuit at a time other than said specified period of time before and after

said frame pulse is generated when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging circuit.

14. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting circuit for detecting a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging circuit for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting circuit; and

a stop controlling circuit for stopping an operation of a circuit connected to a front stage only for a specified period of time before and after a frame pulse is generated when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging circuit.

15. The frame synchronization detecting circuit according to Claim 14, wherein said stop controlling circuit, when canceling a stop of operations of said circuit, cancels said stop of operations of said circuit connected to said front stage after it has canceled a stop of timing of frame synchronization detection operations.

16. A frame synchronization detecting circuit comprising:

a frame synchronization pattern detecting circuit for detecting a predetermined frame synchronization pattern contained in received data having a frame structure;

a hunting state judging circuit for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting circuit; and

an operation stopping circuit for stopping operations of, at least, a part of said frame synchronization detecting circuit only for a specified period of time before and after a frame pulse is generated which indicates a head of a frame containing said received data when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging circuit.